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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/811,152	03/04/1997	YOSHIHARU HIRAKATA	07977/132001	9805

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EXAMINER	
CHOWDHURY, TARIFUR RASHID	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/811,152	HIRAKATA ET AL.	
	Examin r	Art Unit	
	Tarifur R Chowdhury	2871	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *138-165* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *138-165* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 138-143, 145-150, 152-157 and 159 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (Yamazaki), USPAT 5,815,226 in view of Yanagawa et al. (Yanagawa), USPAT 5,734,451.

4. Yamazaki discloses and shows in Figs. 3A and 4A-4B, a liquid crystal display device (col. 1, line 6) comprising:

- a substrate;
- a thin film transistor over the substrate;

- a second interlayer insulating film (315) (applicant's first interlayer insulating film) comprising an organic resin over the thin film transistor;
- a common electrode (316) having a function of black matrix over the first insulating film (315);
- a third interlayer insulating film (317) (applicant's second interlayer insulating film) over the common electrode (316);
- a pixel line and at least one pixel electrode both formed over the second interlayer insulating film (317), the pixel electrode extending from the pixel line;
- a liquid crystal layer over the pixel line and the pixel electrode; wherein the pixel electrode is electrically connected to the thin film transistor through the pixel line; and
- a storage capacitor (319) formed between the pixel line and the black matrix.

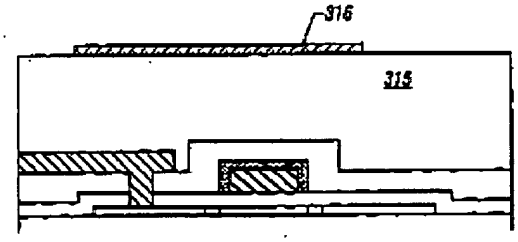

Figure 4A

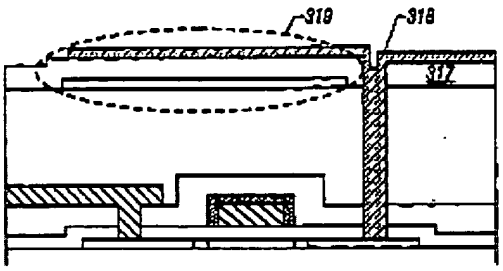

Figure 4B

Yamazaki differs from the claimed invention because Yamazaki does not explicitly disclose that the liquid crystal display device is an in-plane switching type device, i.e., the liquid crystal layer being driven by an electric field formed between the pixel electrode and the common electrode, the electric field having a component parallel with the substrate.

Yanagawa discloses an in-plane switching type liquid crystal display device wherein the liquid crystal layer is driven by a parallel electric field formed between the display electrode (applicant's pixel electrode) and a reference electrode (applicant's common electrode) (col. 1, lines 13-22). Yanagawa further discloses that a liquid crystal display device employing the so-called in-plane switching method allows the viewer to recognize a clear image over a wide range of visual field (col. 1, lines 23-28).

Yanagawa is evidence that ordinary workers in the art of liquid crystal would find the reason, suggestion or motivation for employing in-plane switching method.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the liquid crystal display device of Yamazaki such that the liquid crystal layer is driven by a parallel electric field formed between the

pixel electrode and the common electrode so that the viewers are capable of recognizing a clear image over a wide range of visual field, as per the teachings of Yanagawa.

Accordingly, claims 138 and 153 would have been obvious.

As to claim 146, even though Yamazaki does not explicitly disclose/show the second substrate, since Yamazaki discloses that his invention is related to a liquid crystal display device (col. 1, lines 6-7) and conventional liquid crystal display devices includes two substrates opposed to each other to hold the liquid crystal material there-between, one of ordinary skill in the art of liquid crystal would easily find a reason, suggestion or motivation to employ a second substrate opposed to the first substrate so that it can hold the liquid crystal material there-between when forming a liquid crystal display device.

As to claims 139, 147 and 154, Yamazaki discloses that the pixel electrode has a width in a range of 1000 to 1200 Å, which is equal to 0.1 to 0.12 μm (overlaps the claimed range) (col. 6, line 59).

As to claims 140, 148 and 155, Yamazaki discloses that the third interlayer insulating film (applicant's second interlayer insulating film) is made of an organic resin material and has a relative dielectric constant larger than that of the second interlayer insulating film (applicant's first interlayer insulating film) (col. 6, lines 42-46).

As to claims 141, 149 and 156, Yamazaki discloses that the material for the third interlayer insulating film (applicant's second interlayer insulating film) is not limited to organic resins. Inorganic dielectric films having larger relative dielectric constants can

also be used. Preferably, a silicon-oxide based is used as such inorganic dielectric film (col. 6, lines 49-53).

As to claim 142, Yamazaki discloses that the TFT has a semiconductor layer including a high resistivity region.

As to claims 143, 150 and 157, Yamazaki discloses that the second interlayer insulating film (applicant's first interlayer insulating film) has a thickness in a range of 0.1 to 5.0 μm (col. 6, lines 18-19) and the third interlayer insulating film (applicant's second interlayer insulating film) has a thickness in a range of 0.1 to 0.3 μm (col. 6, lines 40-41).

As to claims 145, 152 and 159, it is clear from figure 4B of Yamazaki that the second interlayer insulating film (315) (applicant's first interlayer insulating film) exhibits excellent flatness and thus serves as a planarization film.

5. **Claims 144, 151 and 158 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view Yanagawa as applied to claims 138-143, 145-150, 152-157 and 159 above and in view of Yamazaki et al., USPAT 5,814,834.**

6. Yamazaki discloses a liquid crystal display device comprising a thin film transistor connected with the pixel electrode and having, as an active layer, a semiconductor layer. See Fig. 4B.

Yamazaki differs from the claimed invention because he does not show that the semiconductor layer is separated into a base and a floating island region.

Yamazaki et al., discloses a thin film transistor having as an active layer, a semiconductor layer that is separated into a base region (107) and a floating island

region (103-106) (Figure 1). Yamazaki et al. further disclose that such an arrangement is advantageous since it decreases a leak current and improve an ON/OFF ratio in a thin film transistor (col. 2, lines 22-31).

Yamazaki et al. is evidence that ordinary workers in the art of liquid crystal display device with thin film transistors would find the reason, suggestion or motivation of using a thin film transistor having as an active layer, a semiconductor layer that is separated into a base region and a floating island region.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the thin film transistor of Yamazaki such that the semiconductor layer is separated into a base region and a floating island region to decrease a leak current and to improve ON/OFF ratio of the thin film transistor, as per the teachings of Yamazaki et al.

Accordingly, claims 144, 151 and 158 would have been obvious.

7. Claims 160-163 and 165 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Yanagawa as applied to claims 138-143, 145-150, 152-157 and 159 above and further in view Kenichi et al., (Kenichi), JP 4-163528

8. Yamazaki differs from the claimed invention because he does not explicitly disclose that the interlayer insulating film comprising a material selected from the group consisting of an organic resin material and an inorganic material.

Kenichi discloses an active matrix liquid crystal display. Kenichi also discloses that by forming a multilayer insulating film where an organic insulating film and an

inorganic insulating film are laminated in order, it is possible to keep off any possible separation at the time of patterning for a transparent electrode (abstract).

Kenichi is evidence that ordinary workers in the art of liquid crystal would find a reason, suggestion or motivation to use a multilayer insulating film that includes an organic resin film and an inorganic film laminated in order.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the second interlayer insulating film of Yamazaki when modified by Yanagawa such that it comprises a material selected from the group consisting of an organic resin material and an inorganic material so that any possible separation during patterning of the transparent electrode is prevented, as per the teachings of Kenichi.

As to claim 161, Yamazaki discloses that the pixel electrode has a width in a range of 1000 to 1200 Å, which is equal to 0.1 to 0.12 μm (overlaps the claimed range) (col. 6, line 59).

As to claim 162, Yamazaki discloses that the material for the third interlayer insulating film (applicant's second interlayer insulating film) is not limited to organic resins. Inorganic dielectric films having larger relative dielectric constants can also be used. Preferably, a silicon-oxide based is used as such inorganic dielectric film (col. 6, lines 49-53).

As to claim 163, Yamazaki discloses that the second interlayer insulating film (applicant's first interlayer insulating film) has a thickness in a range of 0.1 to 5.0 μm

(col. 6, lines 18-19) and the third interlayer insulating film (applicant's second interlayer insulating film) has a thickness in a range of 0.1 to 0.3 μm (col. 6, lines 40-41).

As to claim 165, it is clear from figure 4B of Yamazaki that the second interlayer insulating film (315) (applicant's first interlayer insulating film) exhibits excellent flatness and thus serves as a planarization film.

9. **Claim 164 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view Yanagawa and Kenichi as applied to claims 160-163 and 165 above and further in view of Yamazaki et al., USPAT 5,814,834.**

10. Yamazaki discloses a liquid crystal display device comprising a thin film transistor connected with the pixel electrode and having, as an active layer, a semiconductor layer. See Fig. 4B.

Yamazaki differs from the claimed invention because he does not show that the semiconductor layer is separated into a base and a floating island region.

Yamazaki et al., discloses a thin film transistor having as an active layer, a semiconductor layer that is separated into a base region (107) and a floating island region (103-106) (Figure 1). Yamazaki et al. further disclose that such an arrangement is advantageous since it decreases a leak current and improve an ON/OFF ratio in a thin film transistor (col. 2, lines 22-31).

Yamazaki et al. is evidence that ordinary workers in the art of liquid crystal display device with thin film transistors would find the reason, suggestion or motivation of using a thin film transistor having as an active layer, a semiconductor layer that is separated into a base region and a floating island region.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the thin film transistor of Yamazaki such that the semiconductor layer is separated into a base region and a floating island region to decrease a leak current and to improve ON/OFF ratio of the thin film transistor, as per the teachings of Yamazaki et al.

Accordingly, claim 164 would have been obvious.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tarifur R Chowdhury whose telephone number is (703) 308-4115. The examiner can normally be reached on M-Th (6:30-5:00) Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William L Sikes can be reached on (703) 305-4842. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7005 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

T. Chowdhury
Patent Examiner
Technology Center 2800

TRC
December 12, 2002